Reduce CMOS-multiplexer troubles through proper device selection

CMOS analog multiplexers exhibit problems with output leakage currents and overvoltage-protection circuitry. Here's how to deal with them.

Dick Wilenken, Intersil Inc

A CMOS analog multiplexer (MUX) is basically a channel-selector switch which can interface signal sensors and computers. It provides a number of input channels, which are time-shared onto a common output terminal. A central computer or microprocessor digitally sequences the MUX to "see" one channel at a time. The goal of designers is to pass the sensed signal through this multiplexer with virtually no error terms present. Providing adequate overvoltage protection also presents a challenge. Both objectives can tax designers' ingenuity unless they are familiar with multiplexer anatomy.

Many designers devise unnecessarily complex circuits in their efforts to avoid the substantial level of error terms that can be encountered during the multiplexing operation and to provide overvoltage protection for the CMOS circuitry. But you can save pc-board space, reduce component count and cost, and avoid the possibility of introducing new errors through proper identification of error sources. And adequate circuit self-protection is the result of the proper choice of multiplexing devices.

Output leakage—the major error source

A typical data-acquisition system, extending from sensors to computer, is shown in Fig 1. Here the sensors feed directly into the multiplexer input lines, but this is an idealized case, because

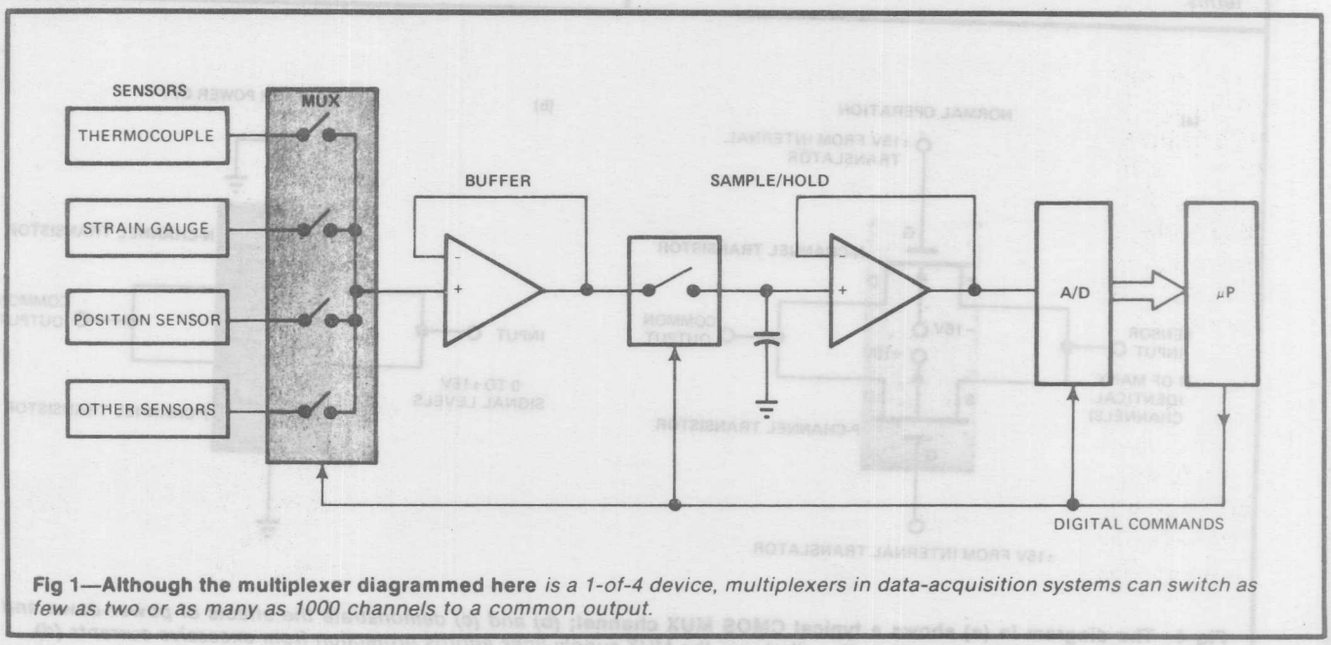


Fig 1—Although the multiplexer diagrammed here *is a 1-of-4 device, multiplexers in data-acquisition systems can switch as few as two or as many as 1000 channels to a common output.*

Identification of error sources reduces component count and cost

most users insert operational amplifiers between the sensors and the MUX inputs. You can eliminate these op amps, however, if you utilize an IC MUX with very low output leakage currents.

Most popular CMOS analog multiplexers have finite ON resistance and leakage currents. Typical of these ICs are the DG506 to DG509 (Siliconix), HI506 to HI509 (Harris) and the IH6116/6208 Series (Intersil).

As noted, the design goal for the system in Fig 1 is to transfer the sensed signal into the sample-and-hold circuit with as little error as possible. Some potential error sources are labeled in Fig 2. One such error source arises from a voltage-divider action between $r_{DS(ON)}$ of a multiplexer ON channel (a consequence of finite channel resistance) and the input impedance of the follower op amp (R_{in}). The signal level at the positive input of the op amp is equal to the sensor voltage times $R_{in}/R_{in}+r_{DS(ON)}$. And the error produced is equal to the ratio of R_{in} to $R_{in}+r_{DS(ON)}$. Because R_{in} (at low frequencies to dc level)=100MΩ and $r_{DS(ON)}$=1 kΩ, the error equals $10^8/10^8+10^3=1/1+10^{-5}$. This set of conditions yields an accuracy of 0.001%; $r_{DS(ON)}$ can range as high as 10 kΩ and still provide 0.01% accuracy. The obvious conclusion to be drawn is that the $r_{DS(ON)}$

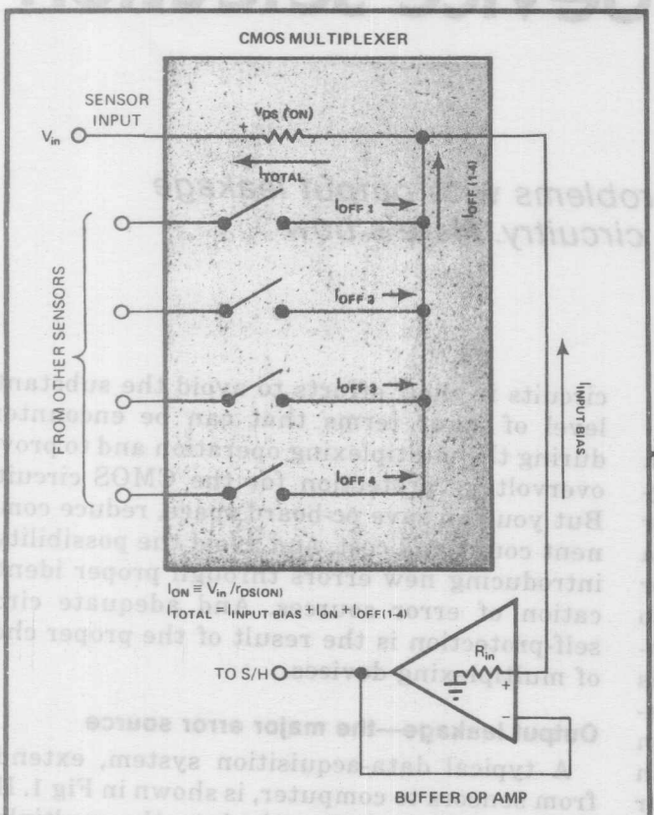


Fig 2—With all but one channel OFF, *this equivalent circuit for the MUX/buffer portion of* ***Fig 1*** *shows potential error terms.*

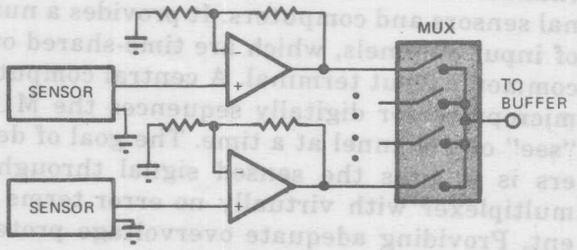


Fig 3—Boosting sensor output levels *can overcome leakage and $r_{DS(ON)}$ errors, but you must pay for the added op amps and the resistors.*

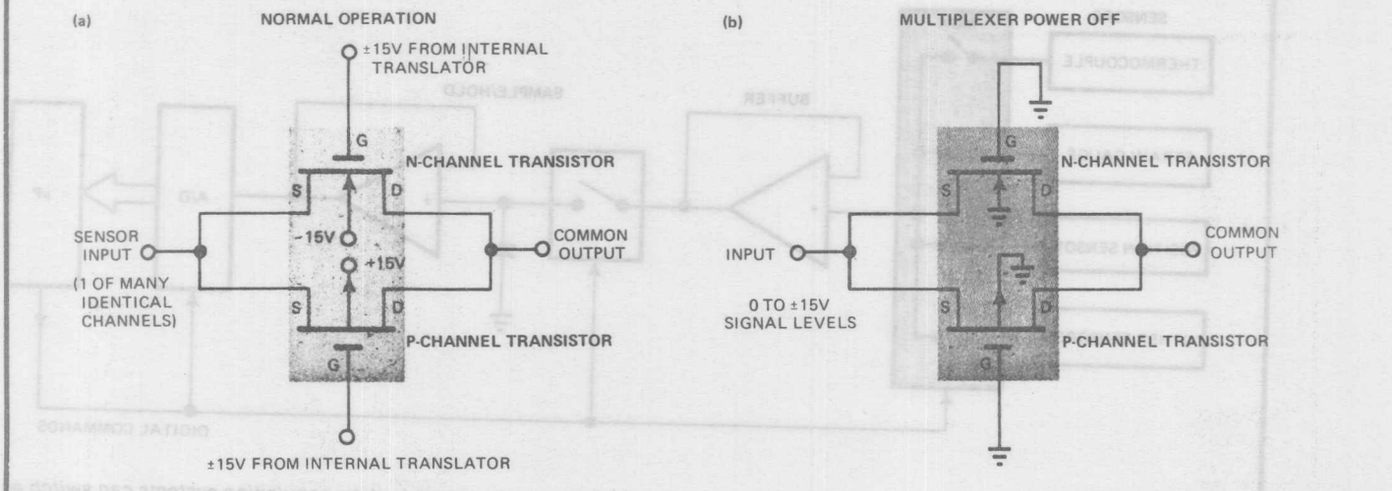


Fig 4—The diagram in (a) shows a typical CMOS MUX channel; *(b) and (c) demonstrate the effects of power-down and overvoltage faults, respectively. Inserting diodes in the MUX supply lines affords protection from excessive currents* ***(d)****.*

of the ON channel is not a very significant factor so long as it is less than 10 kΩ.

A second and much more significant source of multiplexer error stems from I_{TOTAL} (basically total leakage plus input bias current) flowing across $r_{DS(ON)}$. (The total leakage is the sum of the OFF-channel leakage plus the I_{ON} channel leakage.) For example, assume that $I_{OFF(1-4)}$=150 nA, I_{ON}=25 nA and $r_{DS(ON)}$=2 kΩ, all at 125°C. The voltage drop across $r_{DS(ON)}$ is then 175 nA times 2 kΩ, or 350 μV. This 350-μV figure might be considered acceptable if the sensor output were 10V FS. However, thermocouple outputs of 16 mV FS over a 160°C temperature range correspond to 100 μV/°C. Thus, the 350-μV voltage drop across the switch is equivalent to a 3.5°C error—a deplorable level of accuracy. Of course, the same error would be reduced by a factor of approximately 1000 when the ambient temperature drops from 125°C to 25°C: 0.350 μV at 25°C is virtually error-free.

Specifically, the error factors cannot be reduced to $r_{DS(ON)}$ of the ON channel, but rather to $(I_{output\ leakage}+I_{input\ leakage})r_{DS(ON)}$. The currently available DG506 (1-of-16) multiplexers are specified at 500 nA max at 125°C, and $r_{DS(ON)}$ is in the 500Ω range, producing an error term of 250 μV for the multiplexer itself (exclusive of op-amp input bias currents). By comparison, IH6116 parts are rated at 100 nA max at 125°C, with $r_{DS(ON)}$ of 1 kΩ; the maximum error term therefore equals 100 μV, or ±1°C for typical thermocouple sensors.

Dealing with leakage

Fig 3 is a block diagram of a circuit providing a solution to the problem of leakage and $r_{DS(ON)}$ errors. In it, the signal levels are boosted so that the MUX error becomes a much smaller proportion of the multiplexer input signal. But this technique is expensive; the parts count is larger, more pc-board space is used, and new sources of error are introduced: op-amp offsets and temperature drifts.

You can zero the raw offset down to 100 μV with a $0.50 potentiometer. But how do you reduce offset drift?

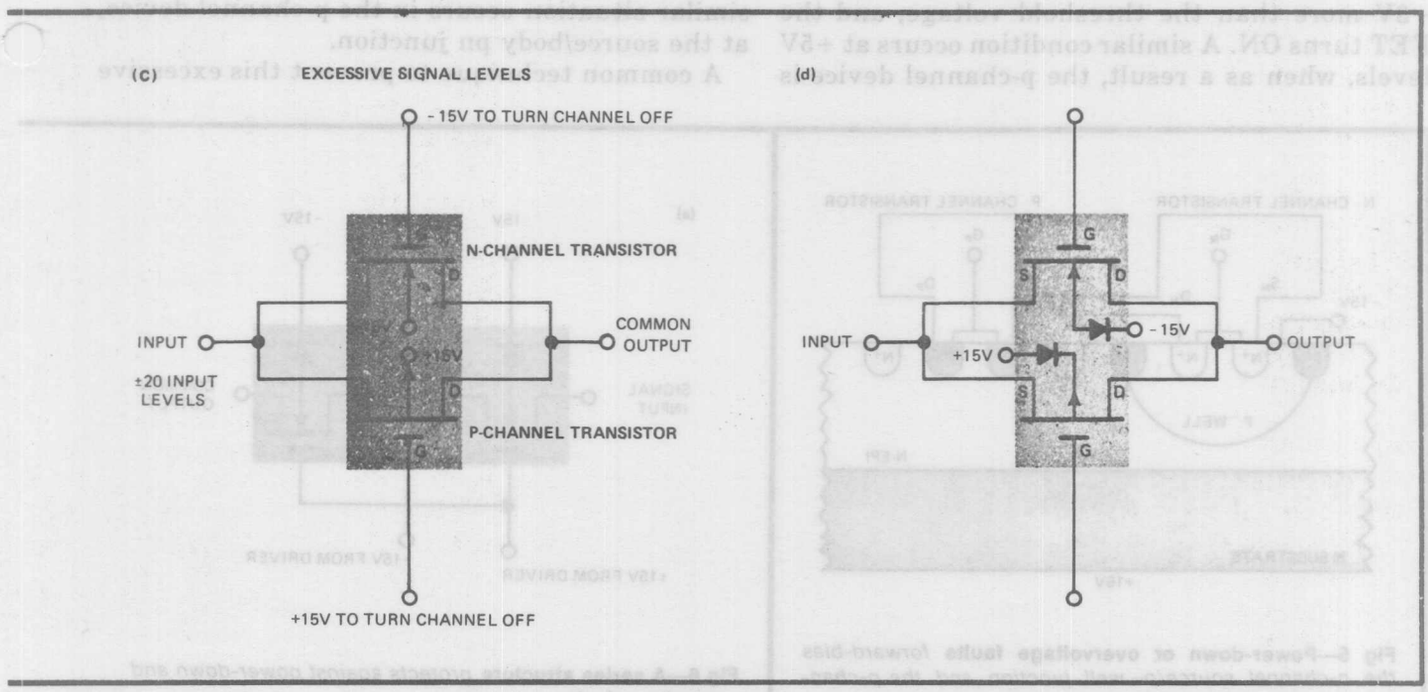
Because the thermocouple scale is 100 μV/°C, the op-amp drift must be no greater than 100 μV/°C to contribute less than 10% error. Therefore, the best solution is to avoid inserting op amps between the sensors and the multiplexer, and to choose instead a multiplexer with significantly lower output leakages.

You might have to spend a few dollars more to obtain a MUX specified at, say, a maximum $I_{D(OFF)} \leq 100$ nA at 125°C. But the alternative is the 16 op amps and all those gain resistors required for 16 channels of low-level sensing. And even if you use 741s, following this approach will cost you at least $4 (16 op amps at $0.25 each). However, if you choose a MUX with the lower leakage specifications, you'll save both money and pc-board space.

Overvoltage fault protection

As noted, CMOS multiplexers are designed to operate as sequential, time-shared multiple switches: When all supplies are correctly operating, only one channel is ON at a time. But when power supplies to a CMOS MUX are turned off, all sorts of damaging effects can occur.

Most of today's IC multiplexers operate from ±15V, GND and perhaps +5V. The sensor signals come from instruments powered by local sup-



Channel ON resistance is not as significant as leakage currents

plies, which are usually independent of the MUX power supplies. When the multiplexer power is down while the signal inputs are active, the majority of today's CMOS multiplexers will not operate sequentially—instead, all channels will be turned ON simultaneously. In that case, one transducer is forced to drive the other transducers via the ON-channel resistances—operation that can be very tough on the sensors. The origin of this problem lies in the design and fabrication techniques currently employed in manufacturing a CMOS multiplexer like the DG506 or IH6116.

A typical CMOS channel circuit is shown in **Fig 4a**. If the sensor input signals are lower than ±15V with MUX power on, no malfunctions occur. But if the sensor signals exceed the levels of the MUX power supplies, or if the multiplexer power is off, the channels are coupled.

Fig 4b depicts a condition where the MUX power is down with sensor signals present. Note that with the power off, the gates and bodies of the parallel n- and p-channel MOSFETs are at ground potential. Because most threshold voltages fall in the range of 1 to 5V, the devices are in the enhancement mode (turned ON) when the signal levels exceed these threshold voltages.

For example, assume that ±5V levels are being switched, with the n-channel $V_{threshold}$ at +2V and the p-channel $V_{threshold}$ at −3V. Thus, for −5V levels, the V_{GS} of the n-channel device equals +5V when the gate is at ground potential; this value is +3V more than the threshold voltage, and the FET turns ON. A similar condition occurs at +5V levels, when as a result, the p-channel device is turned ON. Either situation couples all channels with voltage levels higher than the MOSFET's threshold voltage.

While this coupling phenomenon occurs only with multiplexer power down, a similar situation occurs if the MUX power is at a normal ±15V level and the signal levels exceed ±15V, as happens with voltage spikes. Electrically, this condition is indistinguishable from the previous fault situation. **Fig 4c** shows that for levels in excess of −20V, the n-channel device's V_{GS} equals −15V minus the −20V value (resulting in a final figure of +5V), and the device is enhanced (ON). The opposite condition occurs at +20V, when the p-channel device is ON. In either case, all channels are coupled.

Another harmful condition can occur either when a multiplexer is powered-down or when excessive signal levels are present: Heavy current supplied by the sensors flows into the bodies of the n-channel or p-channel MOSFETs; this current could damage the sensors.

The origin of this problem lies in the junction-isolation technique inherent in the fabrication of CMOS devices. **Fig 5** shows a cross-section of typical CMOS parts. Note that the body of the n-channel device contains the p− well (usually tied to −15V) and that the source-to-body junction is an n+/p− silicon junction that looks like a reverse-biased diode under no-fault operation. Specifically, the n+ source is ≦+15V and ≧−15V when the p− well is tied to −15V. When the −15V level is off, the p− well rides at ground potential, and the source might be forward-biased into the body. The only limits on current flow are the maximum current that the sensor can deliver and the bulk resistance of the substrate. A similar situation occurs in the p-channel device, at the source/body pn junction.

A common technique to prevent this excessive

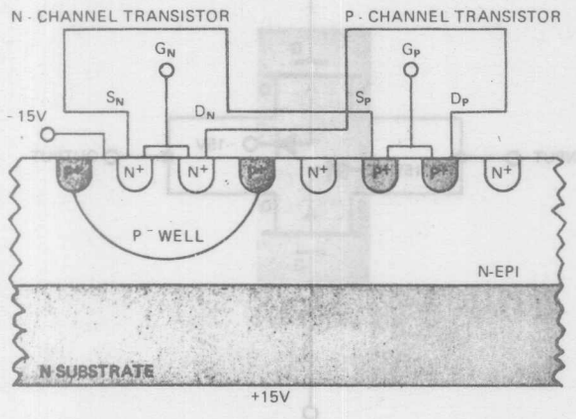


Fig 5—Power-down or overvoltage faults *forward-bias the n-channel source/p− well junction and the p-channel source/n-epi junction.*

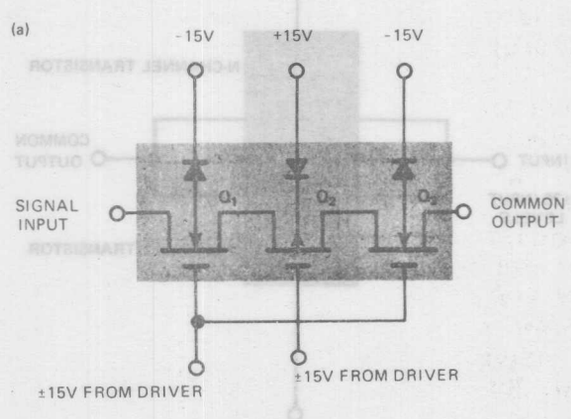


Fig 6—A series structure *protects against power-down and overvoltage faults.*

current flow from the sensor into the MOSFETs' bodies is to add diodes to the multiplexer supply lines, as shown in **Fig 4d.** Addition of these diodes reduces the signal-handling level to +14V (with ±15V supplies). But this factor is somewhat academic because most operational amplifiers have maximum input levels below ±14V (see the follower op amp in **Figs 1** or **2**).

Better protection with a new structure

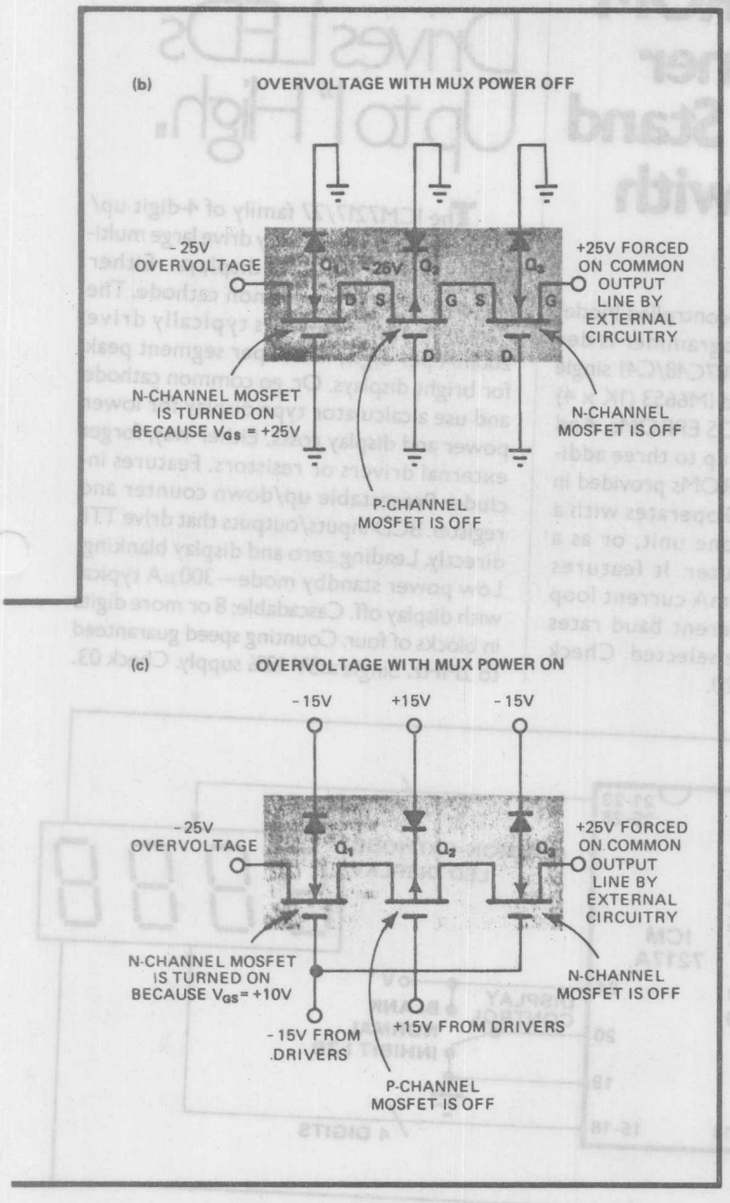
Another family of CMOS multiplexers (Intersil's IH5108 and IH5208), slated for introduction early this year, features an improved fault-protection structure. These devices have a series combination of n- and p-channel MOSFETs instead of the parallel arrangement found in more conventional devices.

The new structures' output-channel configuration is shown in **Fig 6a.** The series-connected n-channel devices are located on either side of the p-channel MOSFET. The IH5108/5208 IC's series-oriented design produces the following electrical characteristics:

- When the ±15V multiplexer power is off, all channels are OFF, rather than being ON as occurs in the parallel output stage in **Fig 4.**
- No current is drawn from the sensors—only leakage current is present.
- All channels remain OFF and draw only leakage currents for ±25V overvoltage inputs, regardless of whether multiplexer power is on or off.

Figs 6b and **6c** show two fault conditions and the performance of the series multiplexers' structure under these conditions. In **Fig 6b,** Q_1 is turned ON by the fault condition, but Q_2 and Q_3 remain OFF. Q_2 and Q_3 share a 50V breakdown, and the device with the lowest leakage has the highest voltage drop across it. The series structure is symmetrical, with an n-channel device on either side of the p-channel MOSFET. Reversing the 25V polarity has no effect, because only one n-channel device will be ON with either polarity in effect; the remaining two devices will always be OFF.

The same conditions exist in **Fig 6c**, with the ±15V MUX power turned on. In this case, the gates are driven to −15V for the n-channel devices and to +15V for the p-channel transistor—corresponding to the OFF-channel condition. The gate drive voltages derive from the on-chip TTL translator circuitry. Again, as in **Fig 6b,** Q_1 is turned ON by the overvoltage; Q_2 and Q_3 are OFF and serve to stand-off the 50V voltage drop.



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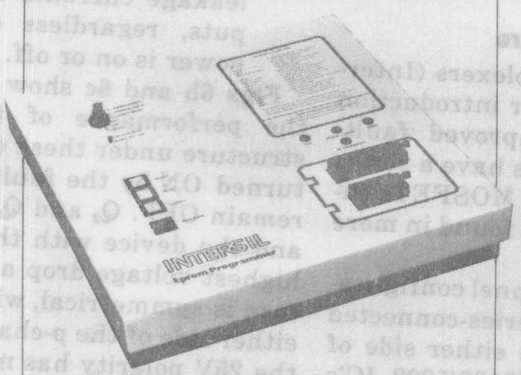

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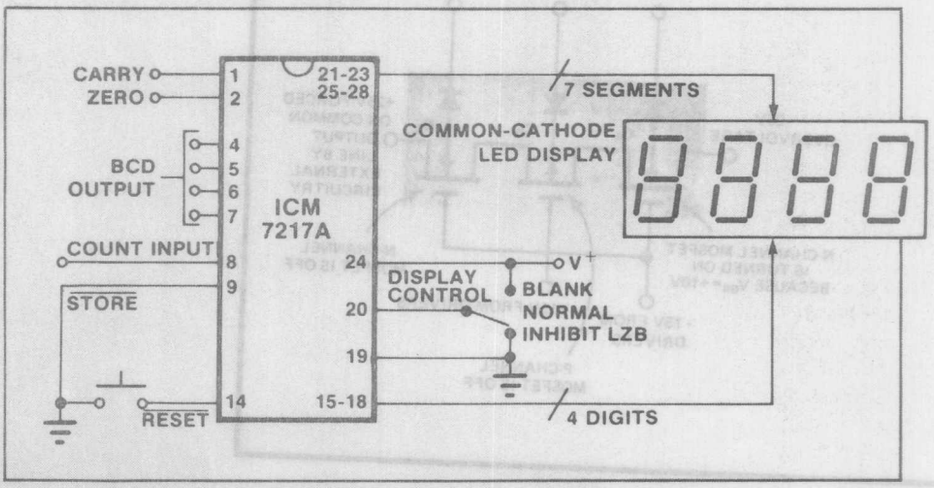

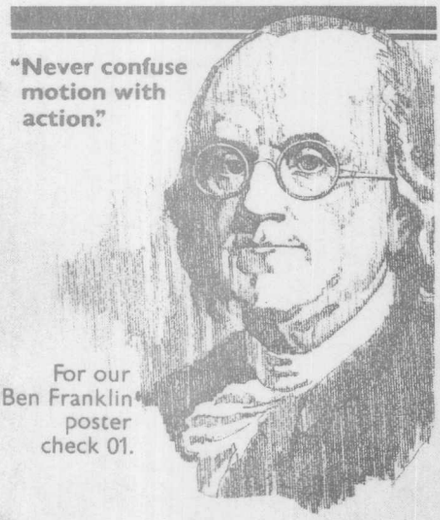

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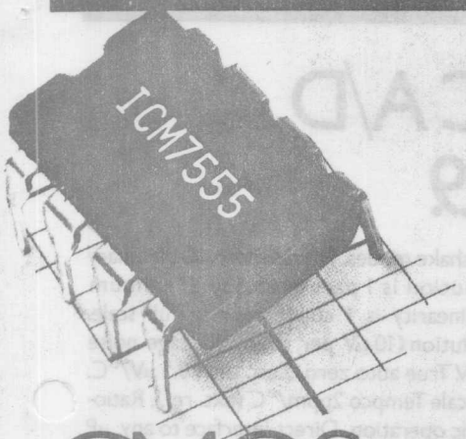

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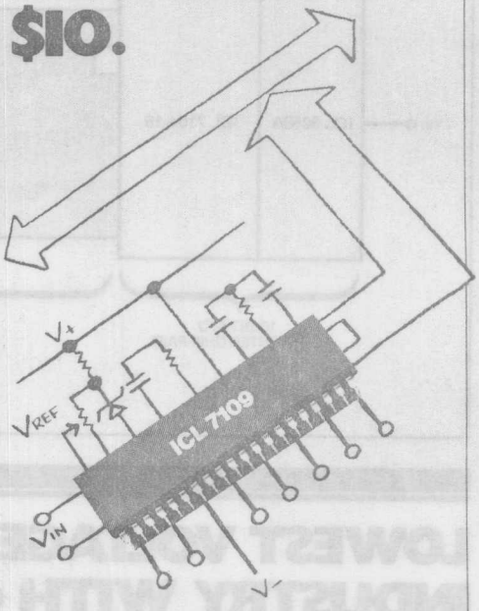

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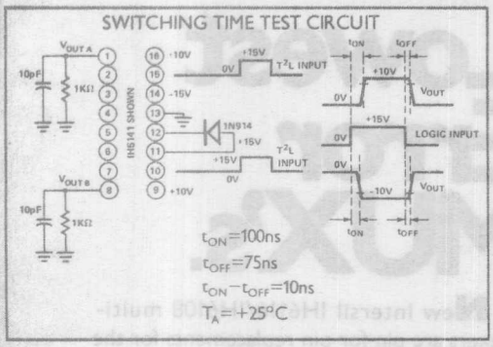

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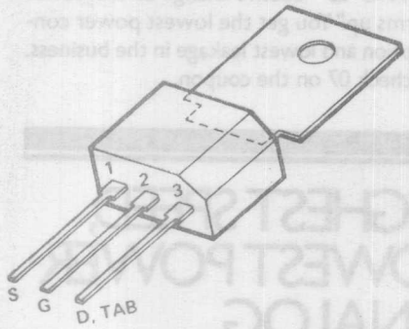

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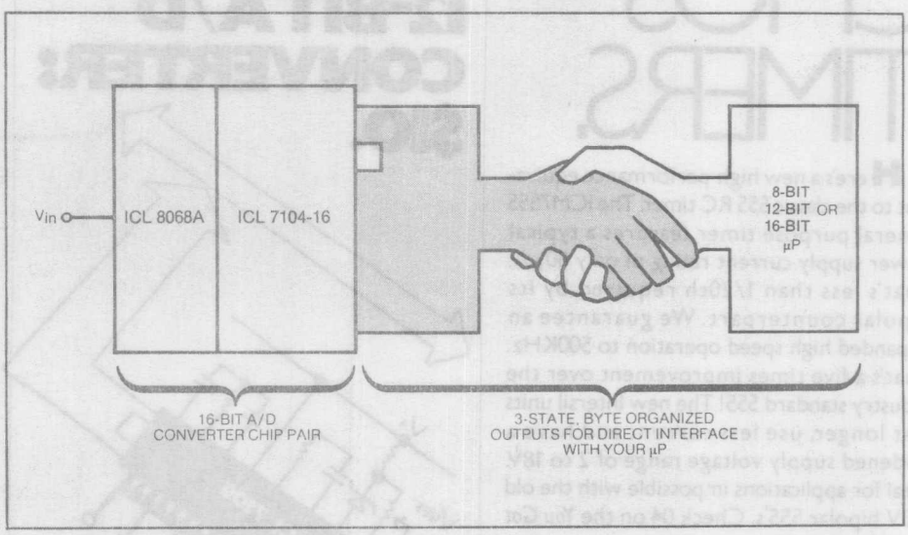

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